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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/530,993	04/12/2005	Masaharu Udagawa	37686	2116
116	7590	10/24/2006		
PEARNE & GORDON LLP 1801 EAST 9TH STREET SUITE 1200 CLEVELAND, OH 44114-3108			EXAMINER CHOE, HENRY	
			ART UNIT 2817	PAPER NUMBER

DATE MAILED: 10/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/530,993

Applicant(s)

UDAGAWA, MASA HARU

Examiner

Henry K. Choe

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 12 April 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,7,8,13-16 and 20 is/are rejected.
- 7) ☒ Claim(s) 3-6,9-12 and 17-19 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 April 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 4/12/05.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Claim Objections***

Claim 8 is objected to because of the following informalities: In line 3 of claim 8, should "bipolar transistors" be --field effect transistors--? Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 13-16 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Amemiya (Fig. 2).

Regarding claims 1 and 2, Amemiya (Fig. 2) discloses an amplifier circuit comprising a plurality of common-emitter amplifier circuits (Q1, Q'1, Q3, Q'3) which are different in voltage gain since the value of resistor 17 is different than the value of resistor 18 and employ bipolar transistors (It should be noted that the transistors Q1, Q'1, Q3, Q'3 are the bipolar transistors.) and formed with an common emitter and common- base cascade connection, and switching means (19) for selecting the plurality of amplifier circuits [(Q1, Q'1, Q3, Q'3); When the switch means 19 is in 19a position, the switch means 19 is selecting the differential amplifier Q3 and Q'3 and when the switch means 19 is in 19b position, the switch means 19 is selecting the differential

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amplifier Q1 and Q'1] and wherein the bases (bases of transistors Q1, Q'1, Q3, Q'3) of the bipolar transistors (Q1, Q'1, Q3, Q'3) are connected in common with each other (bases of transistors Q1 and Q3 are connected to each other and bases of transistors Q'1 and Q'3 are connected to each other) and the switch means (19) are connected to the respective emitter sides of the bipolar transistors (Q1, Q'1, Q3, Q'3).

Regarding claims 13-15, the switch means (19) can be a current source or a transistor or an inverter.

Regarding claim 16, Amemiya (Fig. 2) having bias circuits [(17, 18); It should be noted that the resistors 17 and 18 can be read as the claimed bias circuits since they are affecting the bias voltages of the differential amplifier circuits Q1, Q'1, Q3, Q'3).

Regarding claim 20, Amemiya (Fig. 2) is an amplifier circuit.

### ***Claim Rejections - 35 USC § 103.***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amemiya (Fig. 2).

Amemiya (Fig. 2) discloses all the limitations in the claims except for that the transistors being Field Effect Transistors (FETs). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted well

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known art-recognized equivalent transistors such as FETs in place of the bipolar transistors in the circuit of the Amemiya (Fig. 2) because such a modification would have been considered a mere substitution of art-recognized equivalent transistors.

***Allowable Subject Matter***


Claims 3-6, 9-12 and 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patent numbers (6,515,518; 5,999,044) are the differential amplifiers with the switches.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry Choe whose telephone number is (571) 272-1760.

  
**HENRY CHOE**  
**PRIMARY EXAMINER**

#1174